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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,897	10/30/2003	Harm Peter Hofstee	AUS920030402US1	9220

40412 7590 12/12/2005

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,897	HOFSTEE ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, and 9-10 are rejected under U.S.C. 102(b) as being anticipated by McCrory (International Publication WO 98/19238).

Claim 1. A memory shared by a plurality of heterogeneous processors, comprising: *(Abstract, lines 1-7)*

- the shared memory; *(Abstract, lines 5-7)*
- wherein the shared memory is accessible *(Page 1, lines 25-30 – State that the processors see the same memory space. Page 8, lines 24-25)*
- by one or more first processors that are adapted to process a first instruction set; *(Page 4, lines 23-25 – State that there is a "first type of code designed to run on a first type of processor or family of processors)*
- and wherein the shared memory is accessible *(Page 1, lines 25-30 – State that the processors see the same memory space. Page 8, lines 24-25)*
- by one or more second processors that are adapted to process a second instruction set. *(Page 4, lines 25-27 – State that there is a "second type of code designed to run on a second type of processor or family of processors)*

Claim 2. The shared memory as described in claim 1 further comprising: a memory map corresponding to the shared memory, wherein the memory map is shared between the first processors and the second processors. *(Page 13,*

lines 23-25 – State that each physical location in the memory space has an address which is common between the processors, which is the definition of a memory map)

Claim 3. The shared memory as described in claim 2 further comprising: an operating system that operates on one of the first processors, the first processor controlling the memory map. *(Page 13, lines 19-25 – State that an operating system controls the processors which see the same memory space which is common between all the processors)*

Claim 4. The shared memory as described in claim 1 wherein each second processor further comprises:

- a synergistic processing unit; *(Page 8, lines 18-19 – Intel Pentium 133 MHz and Intel X86 are examples of microprocessors)*
- a local storage; *(Page 13, line 2 – Mentions a memory cache, which is a type of local storage)*
- and a memory management unit, the memory management unit including a direct memory access controller. *(Page 13, lines 26-28 – Declares that all the processors are controlled by a heterogeneous symmetric multi-processing operating system)*

Claim 5. The shared memory as described in claim 4 wherein at least one of the second processors use the direct memory access controller to access the shared memory. *(Page 14, line 3 – States that the second processor can utilize the controller)*

Claim 9. The shared memory as described in claim 1 wherein the memory, the first processors, and the second processors are included on one substrate. *(Abstract, lines 1-3 – State that the family of processors are on a single platform)*

Claim 10. The shared memory as described in claim 1 wherein the shared memory, the first processors, and the second processors are connected using an on chip coherent multi-processor bus. *(Page 12, lines 23-26 – State that an*

"implementation communication mechanism acts as a data and control bus for interfacing processor boards to a shared memory")

3. Claims 11-13 are rejected under U.S.C. 102(b) as being anticipated by Parrish et. al (US Patent 5,117,350)

Claim 11. A method for sharing a memory between a plurality of heterogeneous processors, said method comprising: *(Column 4, lines 36-38)*

- receiving a memory request; *(Column 5, lines 13-17 – State that there are requests for allocation of memory)*
- allocating a first memory partition on the shared memory that corresponds to the memory request, the first memory partition accessible by one or more first processors that are adapted to process a first instruction set; and assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set. *(Column 16, lines 34-46 – Declare multiple memory partitions that all have separate processors and nodes that communicate and give instructions)*

Claim 12. The method as described in claim 11 further comprising: managing the first memory partition and the second memory partition using a common memory map. *(Column 12, lines 67-68 and Column 13, lines 1-2 – State that there are two partitions that are mapped)*

Claim 13. The method as described in claim 12 wherein one of the first processors includes an operating system whereby the first processor controls the common memory map. *(Column 9, lines 14 – Define a memory map that needs to be controlled by some sort of processor)*

Claim 17. The method as described in claim 11 wherein at least one of the second processors uses a direct memory access controller for accessing the shared memory. *(Column 6, lines 27-29)*

Claim 18. A computer program product stored on a computer operable media for sharing a memory between a plurality of heterogeneous processors, said computer program product comprising: *(Column 3, lines 7-25)*

- means for allocating a first memory partition on the shared memory that corresponds to the memory request, the first memory partition accessible by one or more first processors that are adapted to process a first instruction set; and means for assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set. *(Column 16, lines 34-46 – Declare multiple memory partitions that all have separate processors and nodes that communicate and give instructions)*

Claim 19. The computer program product as described in claim 18 further comprising: means for managing the first memory partition and the second memory partition using a common memory map. *(Column 12, lines 67-68 and Column 13, lines 1-2 – State that there are two partitions are mapped)*

Claim 20. The computer program product as described in claim 19 wherein one of the first processors includes an operating system whereby the first processor controls the common memory map. *(Column 9, lines 14 – Define a memory map that needs to be controlled by some sort of processor)*

Claim 24. The computer program product as described in claim 18 wherein at least one of the second processors uses a direct memory access controller for accessing the shared memory. *(Column 6, lines 27-29)*

Claim 25. A memory shared by a plurality of heterogeneous processors, comprising: *(Column 4, lines 28-31)*

- the memory, wherein the memory includes one or more non-private storage areas, the non-private storage areas corresponding to one or more second processors that are adapted to process a second instruction set and access the memory; *(Column 10, lines 34-40 –*

Declare that there is the Remote Global Memory that is dedicated to multiple nodes)

- and wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set and access the memory. *(Column 16, lines 34-46 – Declare multiple memory partitions that all have separate processors and nodes that communicate and give instructions)*

Claim 26. The shared memory as described in claim 25 wherein each second processor further comprises:

- synergistic processing logic which uses private storage, the private storage not included in the shared memory; *(Column 14, lines 50-63 – State that there are partitions that are logically allocated within the system address space)*
- and memory management logic for directly accessing the shared memory. *(Column 1, lines 36-39 – Declares a memory control logic that accesses data from shared memory)*

Claim 27. The shared memory as described in claim 25 further comprising: memory mapping logic that corresponds to the shared memory, wherein the memory mapping logic is shared between the first processors and the second processors. *(Column 12, lines 43-50 – Declare that there is a hardware routing logic that gets information from the entries in the partition RAMs (from different processors), and address translation is done)*

Claim 28. The shared memory as described in claim 27 further comprising: an operating system that operates on one of the first processors, the first processor controlling the memory mapping logic. *(Column 9, lines 14 – Define a memory map that needs to be controlled by some sort of processor. Naturally, the logic is also controlled by the processor if the map itself is also controlled)*

Claim 29. The shared memory as described in claim 25 wherein one of the first processors configures each of the non-private storage areas. *(Column 10, lines 34-40 – State that the Remote Global Memory can be configured)*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C.103(a) as being unpatentable over McCrory as applied to claims 1 and 4 above, further in view of Parrish et al. (US Patent 5,117,350).

McCrory teaches the limitations of claims 1 and 4 for the reasons above.

McCrory's invention differs from the claimed invention in that there is no specific reference dividing the local memory.

McCrory fails to teach claim 6, which states "the local storage is divided into a private storage and a non-private storage". However, Parrish's invention discloses a 'local or private memory space" (column 9, lines 51-52). Parrish's invention also discloses a "shared global memory", which functions as a non-private memory (column 7, line 33). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Heterogeneous System" of McCrory and Parrish's "Memory Address Mechanism" before him at the time the invention was made, to make use of the a local memory divided into private and non-private parts, in order to provide the computer with faster and more efficient access to the memory.

5. Claim 7 is rejected under 35 U.S.C.103(a) as being unpatentable over McCrory as applied to claims 1, 4 and 6 above, further in view of Parrish et al. (US Patent 5,117,350).

McCrory teaches the limitations of claims 1, 4 and 6 for the reasons above.

McCrory's invention differs from the claimed invention in that there is no specific reference to the non-private storage in reference to the shared memory.

McCrory fails to teach claim 7, which states "The shared memory as described in clam 6 wherein the non-private storage is included in the shared memory." However, Parrish's invention discloses that "Remote Global Memory can be configured as being dedicated to each node, or areas can be assigned as common or shared areas" (Column 10, lines 34-37). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Heterogeneous System" of McCrory and Parrish's "Memory Address Mechanism" before him at the time the invention was made, to make use of the a include the non-private storage in the shared memory in order to give more options for accessibility to the memories, thereby making the system more efficient.

6. Claims 8, 14, and 21 are rejected under 35 U.S.C.103(a) as being unpatentable over McCrory as applied to claims 1, 11, and 18-19 above, further in view of Brown (NPL Doc "The Design of ARMphetamin 2", by Julian Brown – henceforth known as "Brown").

McCrory teaches the limitations of claims 1, 11, and 18-19 for the reasons above.

McCrory's invention differs from the claimed invention in that there is no specific reference to any of the regions mentioned in the said claims.

McCrory fails to teach claims 8, 14, and 21, which state "the memory map includes a plurality of regions, wherein at least one of the regions is selected from the group consisting of

an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region. However, Brown discloses an external system memory region (Page 1, line29), a local storage aliases region (Page 6, line 16), a TLB region (Page 2, line 26), an MFC region (Page 5, lines 1-4), an operating system region (Page 10, line 6), and an I/O devices region (Page 2, line 32), which all select at least one of the regions from a memory map (Page 1, lines 23-24). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Heterogeneous System" of McCrory and Brown's "System" before him at the time the invention was made, to make the memory map include a plurality of regions, wherein at least one of the regions is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region, in order to be able to make the memory totally accessible by other heterogeneous processors.

7. Claim 13 is rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claims 11 and 12 above, further in view of McCrory (WO 98/19238).

Parrish teaches the limitations of claims 11 and 12 or the reasons above.

Parrish's invention differs from the claimed invention in that there is no specific reference to a memory map.

Parrish fails to teach claim 13, which states "The method as described in claim 12 wherein one of the first processors includes an operating system whereby the first processor controls the common memory map." However, McCrory's invention discloses that "each physical location in the memory space has an address which is common between the processors, which is the definition of a memory map (Page 13, lines 23-25). It would have been obvious to

one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and McCrory's "Heterogeneous System" before him at the time the invention was made, to allow a first processor to control the common memory map in order to have the primary device maintain control of the mapping for accuracy and consistency.

8. Claim 15 is rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claim 11 above, further in view of McCrory (WO 98/19238).

Parrish teaches the limitations of claim 11 for the reasons above. Parrish also teaches that a processor is a Power PC, when he discloses the "Motorola chip" (Column 3, lines 7-25).

Parrish's invention differs from the claimed invention in that there is no specific reference to the synergistic processing unit.

Parrish fails to teach claim 15, which states "The method as described in claim 11 wherein at least one of the first processors is a Power PC and wherein at least one of the second processors is included in a synergistic processing unit." However, McCrory's invention discloses the "Intel Pentium" 133 MHz and the "Intel X86", which are examples of microprocessors (Page 8, lines 18-19). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and McCrory's "Heterogeneous System" before him at the time the invention was made, to state that a synergistic processing unit could be utilized, since microprocessors are the commonly used devices for computing.

9. Claim 16 is rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claims 11 and 15 above, further in view of McCrory (WO 98/19238).

Parrish teaches the limitations of claims 11 and 15 for the reasons above.

Parrish's invention differs from the claimed invention in that there is no specific reference to the synergistic processing unit.

Parrish fails to teach claim 16, which states "The method as described in claim 15 wherein the shared memory corresponds to the synergistic processing unit." However, McCrory's invention discloses the "Intel Pentium" 133 MHz and the "Intel X86", which are examples of microprocessors (Page 8, lines 18-19). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and McCrory's "Heterogeneous System" before him at the time the invention was made, to state that a synergistic processing unit could be utilized, since microprocessors are the commonly used devices for computing.

10. Claim 22 is rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claim 18 above, further in view of McCrory (WO 98/19238).

Parrish teaches the limitations of claim 18 for the reasons above. Parrish also teaches that a processor is a Power PC, when he discloses the "Motorola chip" (Column 3, lines 7-25).

Parrish's invention differs from the claimed invention in that there is no specific reference to the synergistic processing unit.

Parrish fails to teach claim 22, which states "The computer program product as described in claim 18 wherein at least one of the first processors is a Power PC and wherein at least one of the second processors is included in a synergistic processing unit." However, McCrory's invention discloses the "Intel Pentium" 133 MHz and the "Intel X86", which are examples of microprocessors (Page 8, lines 18-19). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and McCrory's

"Heterogeneous System" before him at the time the invention was made, to state that a synergistic processing unit could be utilized, since microprocessors are the commonly used devices for computing.

11. Claim 23 is rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claims 18 and 22 above, further in view of McCrory (WO 98/19238).

Parrish teaches the limitations of claims 18 and 22 for the reasons above.

Parrish's invention differs from the claimed invention in that there is no specific reference to the synergistic processing unit corresponding to shared memory.

Parrish fails to teach claim 23, which states "The computer program product as described in claim 22 wherein the shared memory corresponds to the synergistic processing unit." However, McCrory's invention discloses the "Intel Pentium" 133 MHz and the "Intel X86", which are examples of microprocessors (Page 8, lines 18-19). Also, McCrory states that "a shared memory may store data and applications programs for use by one or more processors (Page 8, lines 24-25). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and McCrory's "Heterogeneous System" before him at the time the invention was made, to state that a synergistic processing unit could be utilized and correspond to shared memory, since microprocessors are the commonly used devices for computing and referencing the shared memory would allow for convenient and fast data retrieval.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER